What is claimed is:

1. A semiconductor die, comprising:

a substrate;

an integrated circuit supported by the substrate, wherein the integrated circuit includes a test domain having a test voltage and a reference domain having a reference voltage; and

a measurement circuit supported by the substrate, wherein the measurement circuit is operatively connected to the reference domain and the test domain to measure a difference between the test voltage and the reference voltage.

2. The semiconductor die of claim 1, wherein the test domain is a first ground connection of the integrated circuit, and wherein the reference domain is a second ground connection of the integrated circuit.

3. The semiconductor die of claim 1, wherein the integrated circuit includes a switching logic circuit connected to the test domain.

4. The semiconductor die of claim 1, wherein the measurement circuit includes a peak detector.

5. The semiconductor die of claim 1, wherein the measurement circuit includes a comparison circuit.

6. A semiconductor die, comprising:

a substrate;

an integrated circuit supported by the substrate, wherein the integrated circuit includes a test domain having a test voltage and a reference domain having a reference voltage; and

a measurement circuit including an analog-to-digital converter supported by the substrate, wherein the measurement circuit is operatively connected to the reference domain and the test domain to measure a difference between the test voltage and the reference voltage.

7. An integrated circuit package, comprising:

a plurality of leads;

a substrate electrically connected to the plurality of leads by a plurality of wire bonds; and

an integrated circuit supported by the substrate, wherein the integrated circuit includes:

a test domain having a test voltage and a reference domain having a reference voltage; and

a measurement circuit supported by the substrate, wherein the measurement circuit is operatively connected to the reference domain and the test domain to measure the difference between the test voltage and the reference voltage.

8. The integrated circuit package of claim 7, wherein the test domain is a first ground connection of the integrated circuit, and wherein the reference domain is a second ground connection of the integrated circuit.

9. The integrated circuit package of claim 7, wherein the integrated circuit includes a processor connected to the test domain.

10. The integrated circuit package of claim 7, wherein the integrated circuit includes a memory array connected to the test domain.

11. The integrated circuit package of claim 7, wherein the integrated circuit includes an output driver connected to the test domain.

12. A circuit board, comprising:
a conductive layer; and
an integrated circuit package, comprising:
a plurality of leads, wherein at least one of the plurality of leads is connected to the conductive layer;
a substrate electrically connected to the plurality of leads by a plurality of wire bonds; and
an integrated circuit supported by the substrate, wherein the integrated circuit comprises:
a test domain having a test voltage and a reference domain having a reference voltage; and
a measurement circuit supported by the substrate, wherein the measurement circuit is operatively connected to the reference domain and the test domain to measure the difference between the test voltage and the reference voltage.

13. The circuit board of claim 12, wherein the test domain is a first ground connection of the integrated circuit, and wherein the reference domain is a second ground connection of the integrated circuit.

14. The circuit board of claim 12, wherein the integrated circuit includes a processor connected to the test domain.

15. The circuit board of claim 12, wherein the integrated circuit includes a memory array connected to the test domain.

16. A memory circuit module, comprising:

a circuit board having a conductive layer;

a first memory integrated circuit package connected to the conductive layer; and

a second memory integrated circuit package, comprising:

a plurality of leads, wherein at least one of the plurality of leads is connected to the conductive layer;

a substrate electrically connected to the plurality of leads by a plurality of wire bonds; and

an integrated memory circuit supported by the substrate, wherein the integrated memory circuit comprises:

a test domain having a test voltage and a reference domain having a reference voltage; and

a measurement circuit supported by the substrate, wherein the measurement circuit is operatively connected to the reference domain and the test domain to measure the difference between the test voltage and the reference voltage.

17. The memory circuit module of claim 16, wherein the measurement circuit includes a peak detector.

18. The memory circuit module of claim 16, wherein the measurement circuit includes an analog-to-digital converter.

19. The memory circuit module of claim 16, wherein the measurement circuit includes a comparison circuit.

20. A computer system, comprising:

a processor circuit card including a memory bus; and

a memory circuit module connected to the memory bus, the memory circuit module comprising:

a circuit board having a conductive layer;

a first memory integrated circuit package connected to the conductive layer; and

a second memory integrated circuit package, comprising:

a plurality of leads, wherein at least one of the plurality of leads is connected to the conductive layer;

a substrate electrically connected to the plurality of leads by a plurality of wire bonds; and

an integrated memory circuit supported by the substrate, wherein the integrated memory circuit comprises:

a test domain having a test voltage and a reference domain having a reference voltage; and

a measurement circuit supported by the substrate, wherein the measurement circuit is operatively connected to the reference domain and the test domain to measure the difference between the test voltage and the reference voltage.

21. A ground bounce measurement system, comprising:

a substrate;

an integrated circuit supported by the substrate, wherein the integrated

circuit includes a test domain having a test voltage and a reference domain having a reference voltage; and

a measurement circuit supported by the substrate, wherein the measurement circuit includes a data acquisition system, wherein the measurement circuit is operatively connected to the reference domain and the test domain to measure the difference between the test voltage and the reference voltage, and wherein the difference is acquired by the data acquisition system.

22. The ground bounce measurement system of Claim 21, wherein the test domain is a first ground connection of the integrated circuit, and wherein the reference domain is a second ground connection of the integrated circuit.

23. The ground bounce measurement system of claim 21, wherein the measurement circuit includes a peak detector.

24. The ground bounce measurement system of claim 21, wherein the measurement circuit includes an analog-to-digital converter.

25. The ground bounce measurement system of claim 21, wherein the measurement circuit includes a comparison circuit.

26. A ground bounce measurement system, comprising:

a substrate;

an integrated circuit supported by the substrate, wherein the integrated circuit includes a test domain having a test voltage and a reference domain having a reference voltage; and

a measurement circuit supported by the substrate, wherein the measurement circuit includes a data acquisition system, wherein the measurement circuit is operatively connected to the reference domain and the test domain to measure a

plurality of differences between the test voltage and the reference voltage, and wherein the plurality of differences is acquired by the data acquisition system.

27. The ground bounce measurement system of claim 26, wherein the measurement circuit includes an analog-to-digital converter.

28. The ground bounce measurement system of claim 26, wherein the measurement circuit includes a comparison circuit.

29. The ground bounce measurement system of claim 26, wherein the measurement circuit includes a digital-to-analog converter.

30. The ground bounce measurement system of Claim 26, wherein the plurality of differences are read from the data acquisition system by a computer terminal.

31. A method of forming a semiconductor die, comprising:

forming an integrated circuit supported by a substrate, wherein forming the integrated circuit includes forming a test domain having a test voltage and forming a reference domain having a reference voltage; and

forming a measurement circuit supported by the substrate, wherein forming the measurement circuit includes forming a connection to the reference domain and the test domain to enable measuring a difference between the test voltage and the reference voltage.

32. The method of claim 31, wherein forming the integrated circuit includes forming a first ground connection and a second ground connection, and further includes:

connecting the test domain to the first ground connection; and

connecting the reference domain to the second ground connection.

33. The method of claim 32, wherein the method further includes:
forming a switching logic circuit as a part of the integrated circuit; and
connecting the switching logic circuit to the test domain.

34. The method of claim 31, wherein the method further includes forming a comparison circuit in the measurement circuit.

35. The method of claim 31, further including forming an analog-to-digital converter in the measurement circuit.

36. A method of forming an integrated circuit package, comprising:
forming a substrate;
forming a plurality of leads; and
connecting the plurality of leads to an integrated circuit supported by the substrate with a plurality of wire bonds, wherein the integrated circuit includes:
a test domain having a test voltage and a reference domain having a reference voltage; and
a measurement circuit supported by the substrate, wherein the measurement circuit is operatively connected to the reference domain and the test domain to measure the difference between the test voltage and the reference voltage.

37. The method of claim 36, wherein the integrated circuit includes a first ground connection and a second ground connection, further including:
connecting the test domain to the first ground connection; and
connecting the reference domain to the second ground connection.

38. The method of claim 36, further including forming a processor in the integrated circuit, wherein the processor is connected to the test domain.

39. The method of claim 38, further including forming a memory array in the integrated circuit, wherein the memory array is connected to the test domain.

40. The method of claim 39, further including forming an output driver in the integrated circuit, wherein the output driver is connected to the test domain.

41. A method of assembling a circuit board including a conductive layer, comprising:

connecting an integrated circuit package to the conductive layer, further including forming the integrated circuit package, comprising:

forming a plurality of leads, wherein at least one of the plurality of leads is connected to the conductive layer;

forming a substrate electrically connected to the plurality of leads by a plurality of wire bonds; and

forming an integrated circuit supported by the substrate, wherein forming the integrated circuit comprises:

forming a test domain having a test voltage and forming a reference domain having a reference voltage; and

forming a measurement circuit supported by the substrate, wherein forming the measurement circuit includes operatively connecting the measurement circuit to the reference domain and the test domain to enable measuring the difference between the test voltage and the reference voltage; and

connecting a processor circuit package to the conductive layer.

42. The method of claim 41, further including connecting a memory circuit package to the conductive layer.

43. A method of assembling a memory circuit module, comprising:

forming a circuit board having a conductive layer;

connecting a first memory integrated circuit package to the conductive layer; and

connecting a second memory integrated circuit package to the conductive layer, including forming the second memory integrated circuit package, comprising:

forming a plurality of leads, wherein at least one of the plurality of leads is connected to the conductive layer;

forming a substrate electrically connected to the plurality of leads by a plurality of wire bonds; and

forming an integrated memory circuit supported by the substrate, wherein forming the integrated memory circuit comprises:

forming a test domain having a test voltage;

forming a reference domain having a reference voltage; and

forming a measurement circuit supported by the substrate, wherein the measurement circuit is operatively connected to the reference domain and the test domain to measure the difference between the test voltage and the reference voltage.

44. A method of assembling a computer system, comprising:

forming a processor circuit card including a memory bus; and

connecting a memory circuit module to the memory bus, including forming the memory circuit module, comprising:

forming a circuit board having a conductive layer;

forming a first memory integrated circuit package connected to the conductive layer; and

forming a second memory integrated circuit package, comprising:

forming a plurality of leads, wherein at least one of the plurality of leads is connected to the conductive layer;

forming a substrate electrically connected to the plurality of leads by a plurality of wire bonds; and

forming an integrated memory circuit supported by the substrate, wherein forming the integrated memory circuit comprises:

forming a test domain having a test voltage;

forming a reference domain having a reference voltage; and

forming a measurement circuit supported by the substrate, including forming an operative connection to the reference domain and the test domain to enable measuring the difference between the test voltage and the reference voltage.

45. A method of measuring a ground bounce voltage value of an integrated circuit, comprising:

forming the integrated circuit on a substrate, wherein forming the integrated circuit includes forming a test domain having a test voltage and forming a reference domain having a reference voltage;

applying operational power to the integrated circuit;

measuring a difference between the test voltage and the reference voltage using a measurement circuit on the substrate, wherein the measurement circuit includes a data acquisition system, and wherein the measurement circuit is operatively connected to the reference domain and the test domain to measure the ground bounce voltage value of the integrated circuit as the difference between the test voltage and the reference voltage; and

acquiring the difference using the data acquisition system.

46. The method of claim 45, further including:

coupling the test domain to a first ground connection of the integrated circuit; and

coupling the reference domain as a second ground connection of the integrated circuit.

47. The method of claim 45, wherein the method further includes toggling at least one of a plurality of output lines coupled to the integrated circuit.

48. A method of measuring a plurality of ground bounce voltage values of an integrated circuit, comprising:

forming the integrated circuit on a substrate, wherein the integrated circuit includes a test domain having a test voltage and a reference domain having a reference voltage;

applying operational power to the integrated circuit;

measuring the difference between the test voltage and the reference voltage using a measurement circuit on the substrate, wherein the measurement circuit includes a data acquisition system, and wherein the measurement circuit is operatively connected to the reference domain and the test domain to measure the plurality of ground bounce voltage values of the integrated circuit as the difference between the test voltage and the reference voltage over a selected period of time;

acquiring the difference by the data acquisition system; and

repeating measuring the difference and acquiring the difference a selected number of times.

49. The method of claim 48, wherein the method includes toggling at least one of a plurality of output lines coupled to the integrated circuit.